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10/594,542	09/27/2006	Hideki Agari	2271/76931	3779

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EXAMINER	
BUDD, PAUL A	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,542	AGARI ET AL.	
	Examiner	Art Unit	
	PAUL A. BUDD	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/27/2006,4/21/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1, 3** and **7-9** are rejected under 35 U.S.C. 102 (b) as being anticipated by Roberts (US Patent 5,218,222).

Regarding claim **1**, Roberts discloses a semiconductor apparatus [FIG. 2] includes a substrate [FIG. 3; 34] with a pad [FIG. 2; 11], an internal circuitry region [FIG. 2; 26; pull down transistors], and a protection resistance [FIG. 2; 12; column 4 lines 26-27] formed on the substrate [FIG. 3; 34], the semiconductor apparatus comprising:

the pad [11] being connected to a first electrode [the extension of pad over the resistance region 12 that is in contact with square contact suds] of the protection resistance [12] by a wiring [the extension of the pad over the resistance region 12];

the internal circuitry region [26] being connected to a second electrode [the 21 metal over the resistor contact area per FIG. 3] of the protection resistance [12] by a wiring [FIG. 2; the 21 leading from the resistor to the pull down transistors 26]; and

the protection resistance [12] protecting [see paragraph *3* below; as well as inherent to the structure] the internal circuitry region [26] from electrostatic discharging [see paragraph *3* below]; wherein the pad [11] is placed between [directly in-between per FIG. 2] the protection resistance [12] and the internal circuitry region [26].

3. Roberts discloses on column 2 lines 5-10, "The basic component of the output ESD protection circuit of the present invention comprises a low resistance connected in series between an output pad and conventional active output pullup and pulldown drivers". Roberts discloses on column 4 lines 26-27 "Series resistor 12 allows for enhanced ESD protection as it provides good protection to the output pullup and pulldown transistors by attenuating the voltage waveform resulting from an ESD event".

Regarding claim **3**, Roberts discloses a semiconductor apparatus [FIG. 4] includes a substrate [FIG. 3; 34] with a pad [FIG. 2; 11], an internal circuitry region [FIG. 2; 26; diffusion 26 of the pull down transistors], and a protection resistance [12] formed on the substrate [FIG. 3; 34], the semiconductor apparatus comprising:

the pad [11] being connected to a first electrode [extension of pad 11 over the resistance region 12 that is in contact with square contact suds] of the protection resistance [12] by a wiring [the extension of the pad over the resistance region 12];

the internal circuitry region [26] being connected to a second electrode [the 21 metal over the resistor contact area; also shown on FIG. 3; 21 "output node"] of the protection

resistance [12] by a wiring [the 21 leading from the resistor to the pull down transistors 26]; and

the protection resistance [12] protecting [see paragraph *3* below; as well as inherent to the structure] the internal circuitry region [26] from electrostatic discharging [see paragraph *3* above];

wherein a distance [FIG. 2, from *extension of pad 11 over the resistance region 12* to *the edge of diffusion area 26*] between the first electrode [as above] and the internal circuitry region [26, N+ diffusion area of pull down transistors] is greater [it is greater by the distance shown in FIG. 3 between the two vertical contact studs shown by the resistor symbol] than a distance between the second electrode [FIG. 3; 21 "output node"] and the internal circuitry region [diffusion 26 of the pull down transistors].

Regarding claim **7**, Roberts discloses the semiconductor apparatus as claimed in claim **3**, wherein the pad [11] is placed on an insulating layer [FIG. 3; between 33 and 11] on the protection resistance [12].

Regarding claim **8**, Roberts discloses the semiconductor apparatus as claimed in claim **1**, wherein the protection resistance [12] is formed by an impurity diffusion layer [the polysilicon resistor of Roberts contains impurities that inherently must diffuse when subjected to thermal events]. There is no requirement that the protection resistance be

formed in the substrate and therefore the doped (5 ohms) polysilicon semiconductor material anticipates the broadly claimed “impurity diffusion layer”.

Regarding claim **9**, Roberts discloses the semiconductor apparatus as claimed in claim **1**, wherein a protection circuit [FIG. 1; 12 & 14] is formed by the protection resistance [12] and a protection transistor [FIG. 1; 14; pull down transistors 25-26-27-28; column 4 lines 6-12] included in the internal circuitry region [FIG.2; the output pulldown transistors marked by 26].

4. The label “protection” does not structurally distinguish itself over the pull down transistors.

5. Claims **1-2** are rejected under 35 U.S.C. 102 (b) as being anticipated by Usuki Hideki (Japanese Publication number 11-220094).

Regarding claim **1**, Hideki discloses a semiconductor apparatus [FIG. 1-2] includes a substrate [FIG. 2; 1] with a pad [FIG. 1-2; 10a], an internal circuitry region [FIG. 2; to the left of the FIG.], and a protection resistance [FIG. 1-2; 2] formed on the substrate [1], the semiconductor apparatus comprising:

the pad [10a] being connected to a first electrode [FIG. 2; 4] of the protection resistance [2] by a wiring [7b];

the internal circuitry region [as above] being connected to a second electrode [FIG. 2; 3] of the protection resistance [2] by a wiring [7a, 5, 6]; and

the protection resistance [2] protecting [abstract; as well as inherent to the structure] the internal circuitry region [as above] from electrostatic discharging [abstract];

wherein the pad [10a] is placed between [per FIG. 1 and FIG. 4] the protection resistance [2] and the internal circuitry region [as above].

Regarding claim **2**, Hideki discloses the semiconductor apparatus as claimed in claim **1**, wherein a distance [per FIG. 2] between the pad [10a] and the first electrode [4] and a distance between the pad [10a] and the second electrode [3] are substantially the same [per FIG. 2 they are equal].

6. Claims **3-6** and **8-9** are rejected under 35 U.S.C. 102 (b) as being anticipated by Bohm et al. (US Patent 4,757,363).

Regarding claim **3**, Bohm discloses a semiconductor apparatus [FIG. 2-4] includes a substrate [N-type] with a pad [FIG. 2, 12], an internal circuitry region [FIG. 2; 16], and a protection resistance [FIG. 2; 24] formed on the substrate, the semiconductor apparatus comprising:

the pad [FIG. 2; 12] being connected to a first electrode [FIG. 2the 26 over the doped region 24] of the protection resistance [FIG. 2-3; 24; column 3-4] by a wiring [the 26 not over the doped region 24];

the internal circuitry region [FIG. 2 inverter 16; 51, 54, 56; column 5 lines 27-38] being connected to a second electrode [the 28 over the doped region 24] of the protection resistance [24] by a wiring [the 28 not over the doped region 24]; and

the protection resistance [24] protecting [inherent to the structure] the internal circuitry region [as above] from electrostatic discharging [Title; and columns 1-2];

wherein a distance [the length of the resistor 24] between the first electrode [as above] and the internal circuitry region [as above] is greater [by the length of the resistor 24] than a distance between the second electrode [as above] and the internal circuitry region [as above].

Regarding claim **4**, Bohm discloses the semiconductor apparatus as claimed in claim **3**, wherein the substrate [FIG. 2-4; N-type; column 3 lines 3-28] is provided with a guard ring region [FIG. 3-4; cross-section; 34, 36, 38; FIG. 2; plan view; 34, 36, 38] surrounding the pad [12], the internal circuitry region [as above], and the protection resistance [24]; and

distances from two sides [the two opposite vertical sides] of the first electrode [as above] being rectangular [a rectangle of can be drawn to the upper edge of the guard

ring from each side] to the guard ring region [FIG. 3-4; cross-section; 34, 36, 38; FIG. 2; plan view; 34, 36, 38] adjacent to the first electrode [as above] are substantially equal [per FIG. 2; both sides are equidistant to the guard ring].

Regarding claim **5**, Bohm discloses the semiconductor apparatus as claimed in claim **4**, wherein the protection resistance [24] comprises a well region [FIG. 2-3; 24; p+ diffused area] formed in the substrate [N-]; and

distances from the two sides [as above] of the first electrode [26 over 24] to edge portions of the well region [24] adjacent to the first electrode [26 over 24] are substantially equal [Bohm discloses a symmetric geometric relationship between the edges of the first electrode region (26 over 24) and the well region 24 as seen top down on FIG. 2].

Regarding claim **6**, Bohm discloses the semiconductor apparatus as claimed in claim **5**, wherein distances from two edge portions [the outer vertical edges adjacent each electrode (the 2 sides above) are equidistant from the guard ring] of the well region [24] to the guard ring region [FIG. 2; 34, 36, 38] adjacent to the well region [24] are substantially equal.

Regarding claim **8**, Bohm discloses the semiconductor apparatus as claimed in claim **1**, wherein the protection resistance [24] is formed by an impurity diffusion layer [FIG. 3; 24; column 3 line 50; column 4 lines 19-22].

Regarding claim **9**, Bohm discloses the semiconductor apparatus as claimed in claim **1**, wherein a protection circuit is formed by the protection resistance [24] and a protection [*paragraph 6* below] transistor [FIG. 1-4; 16] included in the internal circuitry region [FIG. 1-4; 16].

7. The label "protection" does not structurally distinguish itself over either transistor of the inverter circuit 16.

1. Claim **7** is rejected under 35 U.S.C. 102 (b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bohm et al. (US Patent 4,757,363).

Regarding claim **7**, Bohm discloses the semiconductor apparatus as claimed in claim **3**, wherein the pad [12] is placed on an insulating layer [FIG. 3; the shaded area between 22 and 26 or 12] on the protection resistance [24]. The shaded area between 22 and 26 or 12 is obviously "an insulating layer".

Conclusion

2. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Paul Budd/

/Jerome Jackson Jr./

Primary Examiner, Art Unit 2815